REMARKS

Claims 1-14, and 21-26 are all the claims presently pending in the application. Claims 15-20 have been withdrawn from consideration pursuant to the previously filed Response to Restriction Requirement, and are hereby cancelled without prejudice or disclaimer. Claims 1, 6, 8, and 13 have been amended herein. Claims 21-26 have been added herein. Applicants respectfully traverse these rejections based on the following discussion.

I. The Prior Art Rejections

Claims 1, 3, 5-8, 10 and 12-14 stand rejected under 35 U.S.C.§102(b) as being anticipated by Miremadi et al., hereinafter "Miremadi" (U.S. Patent No. 5,854,507). Claims 1-4, 7-11, and 14 stand rejected under 35 U.S.C.§102(b) as being anticipated by Moresco et al., hereinafter "Moresco" (U.S. Patent No. 5,655,290). Applicants respectfully traverse these rejections based on the following discussion.

A. The Rejection Based on Miremadi and Moresco

The Office Action indicates that Miremadi discloses all of the features of claims 1, 3, 5, 6, 8, 10, 12, and 13 of the claimed invention, but it admits that Miremadi does not explicitly disclose claims 7 and 14. Nonetheless, the Office Action suggests that the features taught in claims 7 and 14 are to be taken as inherent in the device in Miremadi.

Also, the Office Action indicates that Moresco discloses all of the features of claims 1-4, 7-11, and 14 of the claimed invention, but it admits that Moresco does not explicitly disclose

claims 7 and 14. Nonetheless, the Office Action suggests that the features taught in claims 7 and 14 are to be taken as inherent in the device in Moresco.

B. Applicants' Response

As amended, the present application overcomes the rejections based on the cited prior art. Namely, as amended, independent claims 1 and 8 recite, "a gap between a top of said memory chip package and a botrom of an adjacent substrate, wherein said connectors have a size sufficient to form a space between said substrates, wherein said space is larger than a height of said memory chip package." By incorporating these further distinctions of having a gap between the top of the memory chip package and the bottom of the adjacent substrate, the present invention is patentably distinct from the cited prior art of record because the cited prior art, specifically, Miremadi and Moresco do not teach or suggest incorporating such a feature. In fact, both Miremadi and Moresco are bereft of any language pertaining to having a gap between the memory chip package and an adjacent substrate.

Rather, Miremadi deals with the use of multiple chips on stacked substrates without providing a gap between the memory chip package and the adjacent substrate. In particular, Figures 8 and 9 of Miremadi clearly show that no such gap exists. In fact, in col. 7, lines 36-39 of Miremadi it states, "[t]his relationship is illustrated by FIG.8, which shows that the bottom side 61 of the first substrate has been brought into direct contact with a top side 62 of the IC 63 of the underlying layer." Thus, the claimed invention is patentably distinct from Miremadi.

Similarly, Moresco discloses a wholly unique concept from the claimed invention. In Moresco, multiple chips 110 (not chip packages) are stacked on one another, while the claimed

invention provides for "a single memory chip package mounted on each of said substrates." An important distinction of the claimed invention is the use of chip scale packages 140. A silicon chip is a rectangular segment of a silicon wafer, consisting of a highly-complex active surface, with the bulk of the material being single crystal silicon. Elements of the active surface, important to chip packaging, are primarily the bond pads for electrical connection of the active surface of the chip to the chip package and through the package to the balance of an electronic system.

A chip package, shown in Figure 3 of the claimed invention, serves several purposes. The chip package includes a substrate and bond wires that electrically connect pads on the chip to the solder balls. The chip package provides more robust electrical connection features than chip bond pads for the purpose of testing chips. The chip package transforms the chip into a configuration that can be readily and reliably bonded to the next level of assembly, typically a printed circuit board. The chip package offers physical protection to the chip, both against mechanical damage and chemical attack. A chip package may include one or many chips, but is distinguished from higher-level assemblies, such as the one taught in Moresco, in that it directly contacts the chip silicon.

Burn in of multiple chip packages (e.g., packages having more than one chip such as Moresco) also presents difficulties. Wire bondable and over-molded type packages are not reworkable to remove and replace single defective chips. Thus, any failure of a single chip on a multichip package will result either in rework expense or the discard of the balance of still functional chips on the module. In addition, the functional wiring of a multichip module may make direct testing of a specific function of an individual chip difficult or impossible. Thus,

burn in of a multichip module, such as the module taught in Moresco, may be ineffective, and is contrary to the teaching of the claimed invention.

The claimed invention also discloses the use of chip scale package substrates of a size optimized for small size and socket compatibility to permit burn-in for removal of infant mortality defect prior to stack assembly, which simply is not taught, suggested, demonstrated, or achieved in the device described in either Miremadi or Moresco. In fact, the devices of Miremadi and Moresco suggest an over-molded type package, which may not be reworkable to remove and replace single defective chips. Thus, any failure of a single chip on the multichip package of Miremadi or Moresco may result either in rework expense or the discard of the balance of still functional chips on the module in contrast to the claimed invention.

Moreover, because the claimed invention provides chip scale packages 140 that have been "burned-in" and tested, the invention makes the stack out of structures that are known to be "good" (non-defective). This substantially reduces the defect rate for multichip stack decks. Furthermore, because the claimed invention utilizes chips that are known to be free of defects, many more chips can be utilized per deck (e.g., per substrate level) and the number of decks within the stack can be dramatically increased. This is a feature, which the Miremadi and Moresco devices simply do not possess.

Another novel distinction of the claimed invention over Miremadi and Moresco is that the claimed invention utilizes an optimum number of devices in each stack layer such that the number of independant interconnects required to that layer is minimized. This allows integrated circuit devices to be stacked one upon the other while maintaining a unique pin out for each pin required in the stack. The number of chips commonly addressed in the stack is expanded to an

optimum extent such that the number of memory address interconnects in the stacked module assembly is minimized. In this optimum structure of the claimed invention, the number of data bits addressed in parallel is equal to the system word width. With such a structure as provided by the claimed invention, for each chip added to a deck in the stack structure, an address complement of interconnects needed to expand in the height direction is eliminated. This is a benefit which the devices in Miremadi and Moresco do not possess. In fact, the inventive stacked memory module of the claimed invention uses chip scale packaging technology which minimizes the number of solder interconnects between each single chip device and the module circuit board by allowing common addresses in each stack deck. Therefore, the claimed invention achieves efficiency of manufacture by using chip scale packages rather than chips as building blocks at each deck, amenable to standard burn in practices.

Applicants respectfully submit that Miremadi does not teach or suggest the features defined by amended independent claims 1 and 8, and as such, claims 1 and 8 are patentable over Miremadi. Further, dependent claims 3, 5-7, 10, and 12-14 are similarly patentable over Miremadi not only by virtue of their dependency from patentable independent claims, respectively, but also by virtue of the additional features of the invention they define.

Likewise, Applicants respectfully submit that Moresco does not teach or suggest the features defined by amended independent claims 1 and 8, and as such, claims 1 and 8 are patentable over Moresco. Further, dependent claims 2-4, 7, 9-11, and 14 are similarly patentable over Moresco not only by virtue of their dependency from patentable independent claims, respectively, but also by virtue of the additional features of the invention they define.

Applicants note that all claims are properly supported in the specification and

accompanying drawings, and no new matter is being added. In view of the foregoing, the Examiner is respectfully requested to reconsider and withdraw the rejections.

II. Formal Matters and Conclusion

In view of the foregoing, Applicants submit that claims 1-14 are patentably distinct from the prior art of record and are, in addition to newly added claims 21-26, in condition for allowance. Moreover, the amendments made herein do not narrow the scope of the claims for patentability purposes. In fact, the claim amendments made herein broaden the scope of the present invention due to its applicability in other environments. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time.

Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary. Please charge any deficiencies and credit any overpayments to Attorney's Deposit Account Number 09-0458.

Respectfully submitted,

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